# NOVEL GaAs FET PHASE DETECTOR OPERABLE TO Ka BAND

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## ABSTRACT

A new type of sampling-phase detector using a GaAs FET was developed. This SPD has approximately a 30 mV/rad detection sensitivity at 26.4 GHz with a 19 dBm 100 MHz reference frequency. Detection sensitivity depends on the FET bias voltage in a very unusual way. This paper describes the configuration of the SPD and experimental results of a 50 GHz phase locked oscillator using an oscillator doubler VCO and the SPD.

## INTRODUCTION

There are two general ways of fabricating phase locked oscillators (PLOs). The methods differs according to method that the voltage controlled oscillator (VCO) frequency coincides with the reference frequency. Both methods are described below.

(1) Frequency divider
(2) Sampling phase detector (SPD) (including harmonic mixer)

The microwave frequency divider method uses an analog [1][2] divider or digital prescaler. This circuit is large and has a narrow band width although it is somewhat expensive. The highest operating frequency for commercially available prescalar is 2 GHz which is too low for this application.

The second method (SPD) has the simplest PLO circuit, however, it is useful only up to the C band.

To produce PLOs in frequency ranges as high as 20 to 30 GHz, we successfully developed an SPD which has a new circuit configuration with a GaAs FET and is operative up to Ka band. We also developed a 50 GHz PLO using the SPD and an oscillator doubler VCO.

## SPD (Sampling Phase Detector)

Figure 1 shows a circuit diagram and the phase detection sensitivity characteristics as a function of the frequency. The circuit in Figure 1 is widely used conventional sampling phase detectors which use Schottky barrier diodes (SBDs) and a step recovery diode (SRD). The detection sensitivity is approximately 10 mVp-p (5 mV/rad), which is not high enough to stabilize a PLO.

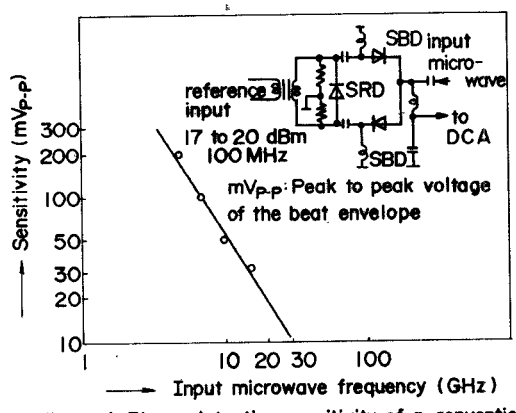


Figure. 1 Phase detection sensitivity of a conventional SPD as a function of the Input microwave frequency

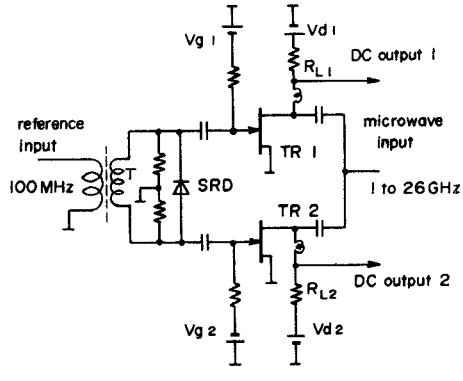


Figure. 2 Equivalent circuit of a balanced-type GaAs FET S.P.D

To gain increased sensitivity, the pulse width of the SRD must be narrowed and the pulse voltage increased. If the load impedance of the SRD is increased, the SRD output pulse width will be narrowed and the pulse voltage will increase, causing the SPD to have a higher sensitivity. We thought that a higher sensitivity might be obtained if the FET, which has high input impedance could be used as a switching device.



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Figure 2 shows an equivalent circuit diagram of the first model of a balanced-type GaAs FET SPD. A positive pulse train is applied to TR1 and a negative pulse train to TR2.

The static theory of operation is shown below in Figures 3 and 4. TR1 is biased over the pinch-off voltage, and TR2 is biased at 0 V, as shown in Figures 3 and 4. The following facts were tested by experiments done with the first model.

(1) Since the operation for TR1 and TR2 are completely different, leakage reference signals on neither drains were effectively cancelled.

(2) The detection sensitivity of TR1 is much higher than TR2.

(3) The phase difference of the two output beat signals generated in the FETs is not always out-of-phase exactly.

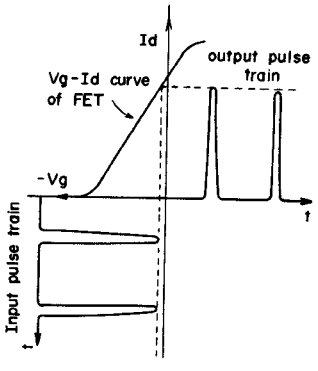


Figure. 3 FET switching operation of positive pulse train ( TR 1 )

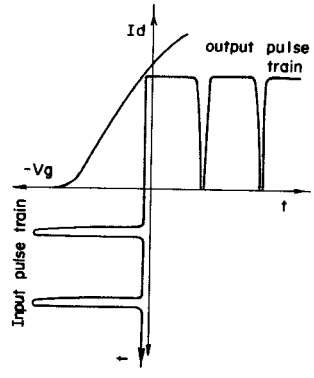


Figure. 4 FET switching operation of negative pulse train ( TR 2 )

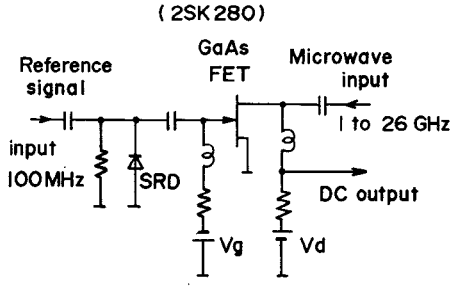


**Figure. 5 Equivalent circuit of the new sampling phase detector**

These results show that a positive pulse must drive an FET gate used in the SPD, and that there is no reason for using a balanced-type GaAs FET SPD. We therefore experimented with the circuit shown in Figure 5. Figure 6 shows an equi-detection sensitivity map of the GaAs FET SPD. The X- and Y-axes show the drain supply voltage and gate voltage, respectively. This map shows the peculiar dependency on bias. There were two peaks, A and B. The sensitivity at point B was approximately 4 to 5 times higher than that at point A.

Figure 7 shows the frequency characteristics of points A and B. This graph showed superiority of detection efficiency at point B.

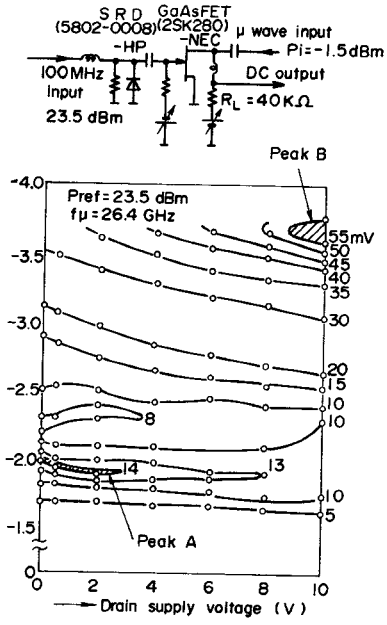


Figure. 6 Equi-detection sensitivity map of the GaAs FET SPD

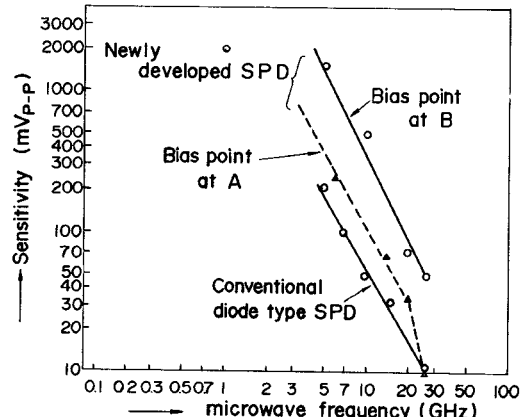


Figure.7 Frequency characteristics of the SPDs

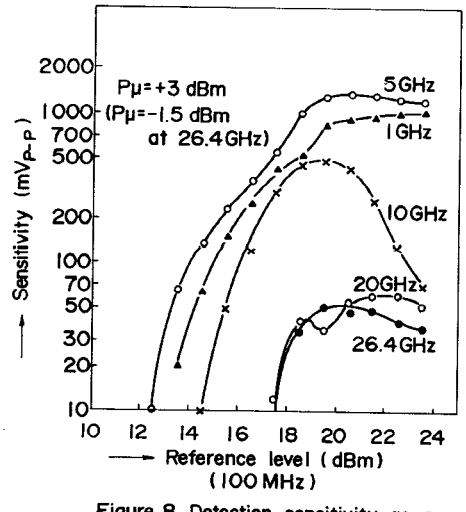


Figure.8 Detection sensitivity as a function of the reference level

Figure 8 and 9 plot detection sensitivity as a function of the reference level and microwave level at point B. The optimum levels for detection sensitivity depended on the frequency. The maximum detection sensitivity of 60 mVp-p (30 mV/rad) was obtained at 26.4 GHz with a 19.5 dBm reference level and a -1.5 dBm microwave level. This was considered large enough to fabricate a PLO.

## APPLICATION TO 50 GHz PLO

We developed a 50 GHz PLO using oscillator doubler type VCO to confirm the feasibility of using the SPD. The VCO consists of a dielectric resonator stabilized Gunn oscillator and a tuning circuit using a varactor diode. Figure 11 shows the oscillation characteristics of the oscillator doubler 50 GHz VCO. The detection sensitivity of the SPD was approximately 25mV/rad. The modulation sensitivity of the VCO was approximately 4 MHz/V. The gain of the DC amplifier was 400, and the hold-in range was 40 MHz.

Figures 10 and 12 show the SPD module and PLO respectively.

The fundamental frequency (25 GHz) was guided to the SPD module by a WRJ-260 wave guide mounted directly opposite the VCO. The 50 GHz, which is multiplied in the Gunn diode, is coupled to the WRJ-500 (fc = 31.4 GHz ) effectively.

## CONCLUSION

We successfully developed a novel sampling phase detector using a GaAs FET. A 50 GHz PLO using an oscillator doubler VCO was fabricated to confirm the validity of the SPD. With this system, highly stable local sources can be easily fabricated for many microwave and millimeter wave radio systems. We plan to analyze the peculiar bias dependency of the detection sensitivity.

## REFERENCES


[1] C. Rauscher;"A 16 GHz GaAs FET Frequency Divider."
1983 IEEE MTT-S DIGEST pp 349-351

[2] D. Kaminsky at el. "A Dual Gate GaAs FET Analog Frequency
Divider." 1983 IEEE MTT-S DIGEST pp 352-354


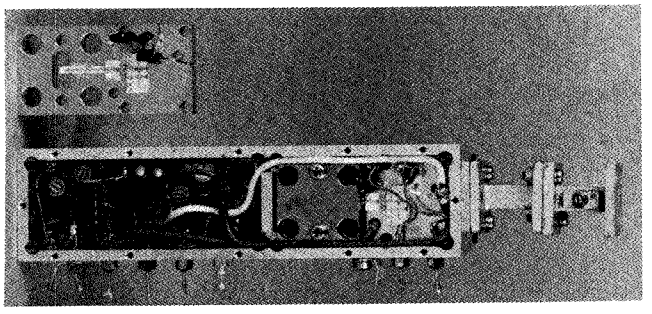

Figure.12 S.P.D module and bottom view of the 50 GHz PLO

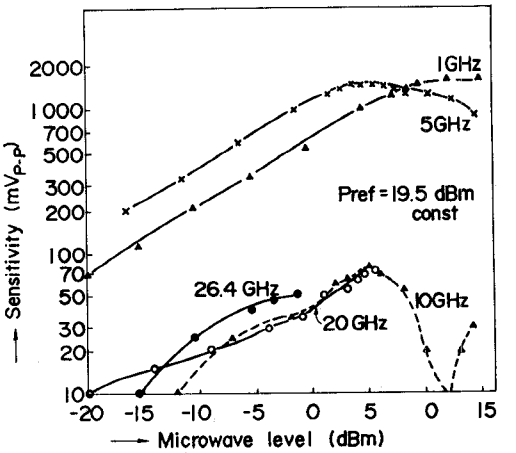


Figure. 9 Sensitivity as a function of microwave level

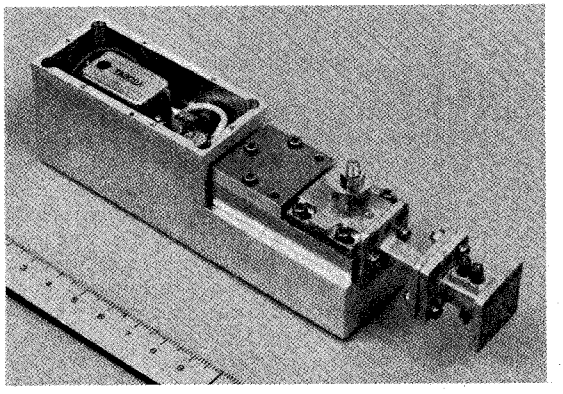

Figure.10 50 GHz PLO

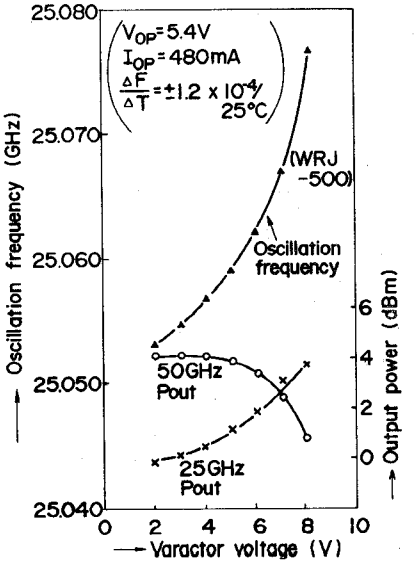


Figure.11 Oscillator doubler VCO tuning characteristics